1100 Seventeenth Street, N.W.

Washington, D.C.

20036

SUBJECT: Possible MSFN Solution to Loss of Bit Synchronization in LM PCM Telemetry - Case 320

DATE: December 15, 1967

FROM: W. J. Benden

AESTRACT

Under certain conditions, PCM telemetry from the Lunar Module (LM) exhibits very low bit transition densities. Since the MSFN derives timing information from these transitions, synchronization, and therefore data, can be lost.

This memorandum describes a possible scheme to cope with the problem. The scheme involves slight modifications of existing equipment and does not influence telemetry from other spacecraft (CSM and S-IVB/IU) which do not exhibit the LM problem.

(NASA-CR-92822) POSSIBLE MSFN SOLUTION TO LOSS OF BIT SYNCHRONIZATION IN LM PCM TELEMETRY (Bellcomm, Inc.) 16 p

N79-72622

Unclas 00/32 11061

(NASA CR OR TMX OR AD NUMBER) (C.

(CATEGORY)

TE TO ME CONTROL NASA

SUBJECT:

Possible MSFN Solution to Loss of Bit Synchronization in LM PCM Telemetry - Case 320

DATE: December 15, 1967

FROM: W. J. Benden

MEMORANDUM FOR FILE

I. <u>Introduction</u>

The PCM bit stream being sent from the LM to the MSFN can exhibit very low bit transition densities. The MSFN receiving station derives its decommutation timing from a VCO loop in the bit synchronizer which is held in lock by telemetry data transitions; it depends on the VCO's memory during periods of no transitions. Of course, if the period of missing bit transitions becomes excessive, the MSFN will lose the required timing for proper decommutation. Although an encoding scheme could be implemented in the LM to circumvent this problem (similar to that used in the CSM) or alternate data stream formats could be chosen, this memorandum addresses the problem from the MSFN modification viewpoint.

Since the timing of the PCM data and the data subcarrier are derived from the same clock in the LM, there exists a coherent relation between the two. This fact leads to a possible conclusion: implement the MSFN so that the MSFN uses this coherent relationship at all times to detect the data. This solution should work well as long as we are receiving LM real-time data; but during playback of recorded CSM data there exists no coherent relation between the subcarrier and the data. Thus, when recorded CSM data is being received in the MSFN, the bit transition density information must be used for detection and the coherent mode can not be employed. As a consequence, operator decisions must be made as to when the coherent mode should be switched in and out. Fortunately, recorded CSM data, S-IVB/IU data (72 Kbs), and LM recorded data (split phase) all contain sufficient bit transition densities, by data format design, to allow the use of MSFN equipment in its present configuration; that is, using the transitions to derive the correct reference for data detection. To cope with the LM problem, it seems that equipment modifications which come into use only when LM real-time data reception is involved would be highly desirable. This memorandum describes such a scheme. The additional equipment essentially operates in parallel with the present system. It is used only for the reception of LM real-time data and only when the transition density of this data falls below a prescribed threshold.

Although detailed descriptions of equipment operation were not available, the functional descriptions (given in Reference 1) seemed sufficient to derive the problem solution.

II. Basic System Operation

Figure 1 illustrates the technique used by the MSFN to demodulate the PCM-C data coming from the LM. The diagram starts in the S-Band receiving equipment where only the 1.024 MHz bi-phase modulated subcarrier appears. The circuitry prior to this point which includes limiting and band pass filtering has been neglected.

The signal spectrum at A (assuming the data to be random) is contained within a $\frac{\sin^2\chi}{x^2}$ envelope centered about

1.024 MHz with nulls at multiples of the data rate away from the subcarrier. The squaring operation removes the modulation and in doing so generates a 2.048 MHz signal which is locked onto by the modulation restrictive phase-lock loop. Thus, after dividing the VCO output by two, a clean reference is provided at point B in Figure 1 for phase detection. PCM-C data appears at point C where it is routed to the bit synchronizer which contains another VCO loop operating at 1/2 the data rate. By differentiating the received waveform, the locations of data transitions are marked and the VCO loop driven into the lock at a frequency directly related to the data rate. After lock the VCO provides the timing information required by the decision circuitry to know when to look at the received waveform to decide if a "One" or "Zero" is present. The reconstructed bit stream then appears at point D. It is the latter VCO which can drop out of synchronism with the spacecraft's commutator when the bit transition density becomes sufficiently low.

III. Possible Solution(s)

Figures 2 and 3 represent possible solution(s) to the timing problem. Figure 2 uses an internal clock in the down counter whereas Figure 3 uses the coherent reference to provide the clock. The method of maintaining synchronism is the same, however, since it is based on the coherent relation between the subcarrier frequency and data rate originating in the LM. As shown in Figure 4, both are derived from the same timing reference in the LM.

A. Basic Operation

The additional circuitry shown in Figure 2 (as well as that shown on Figure 3) is only used when the number of bit transitions fall below a pre-determined value - say "M". Thus, M for example, may equal N/2; where N represents the maximum allowable number of bit intervals without transitions before the MSFN looses synchronization with the spacecraft's commutator. Reference 2 indicates N to be approximately 64.

In referring to Figure 2, the transition detector provides a signal to the down counter which sets it to "M" every time a transition takes place. After being set, the counter counts down towards zero in bit interval steps. The countdown timing is provided by an internal clock. If the count reaches zero (indicating low bit transition density) the system goes into a coherent synchronization mode. That is, at zero state, gate A is enabled on one side and waiting for the 2.048 MHz coherent reference to make it true. Within 0.5 microseconds (one period of the VCO) from the time of the zero state in the down counter, 2.048 MHz pulses begin to appear at the divide by 40 counter. At the end of each 40 count, a pulse appears at the 25.6 KHz VCO loop input; nudging it into step. Note that the original timing reference was derived from the leading edge of the last bit transition; at which time the 25.6 KHz VCO was in synchronization with the spacecraft. The leading edge obtained when the down counter reaches the zero state, M intervals later, is still used as the reference when the 2.048 MHz signal is to be switched into operation. Thus, until the next transition, the timing is based on the coherent spacecraft reference; whatever its time relationship is to the data stream as the counter reaches the zero state. Figure 3 represents the same technique with the exception of the coherent clock being used for the down counter. The timing diagram on Figure 3a aids in the understanding. In retrospect, the descriptions given are only functional, since the details of the various equipments involved were not know at the time of this writing. That is, additional wave shaping devices, time delays, isolation networks, etc., have not been explored in this memorandum.

B. Noise

When only noise is present at the input to the bit synchronizer, there exists the possibility of the decision circuitry producing an apparently valid bit stream at the output. Each transition, be it actual or noise generated, will set the down counter (Figure 2) to M preventing the additional

equipment from being utilized for coherent synchronization. The counter <u>could</u> reach the state of zero if noise caused a transition and throughout the succeeding M intervals caused no transitions. For example, if "M" were 32 and the probability of noise generating a one and a zero were equally likely, then there would be two chances* in 2³² of the system going into a coherent synchronization mode. Possible ways of preventing this very unlikely occurrence might be:

- 1. Utilize the presence of the Frame Synchronization Pattern to allow the transition detector to become operative. Since "ones" could be "zeros" and "zeros" could be "ones" at point C on Tigure 2 both the pattern and its complement can be used to enable the transition detector.
- 2. The additional circuitry can be inhibited until the presently available visual display indicates that data and not noise is entering the bit synchronizer.

IV. CSM and S-IVB Telemetry

The bit synchronizers for the CSM and S-IVB could be modified in the same manner making all three units (LM, CSM. and S-IVB) interchangeable for backup purposes. The modified units accepting telemetry from the CSM and S-IVB will not use the additional circuitry, however, since the bit transition densities are sufficiently high to prevent its employment; including telemetry of CSM recorded data and CSM recorded LM split phase data. Note that the use of a coherent synchronization in the telemetry of CSM recorded data and S-IVB data would be to no avail, since there exists no coherent relationship between the data and the subcarrier. If the counters and additional circuitry were provided for the CSM bit synchronizer, in addition to the access modifications, the telemetry of CSM real-time data could be made coherent by simply setting the down counter to a sufficiently low value of M and inhibiting the set input after the zero state is reached. Since the coherent synchronization should decrease the BER (even during high transition density periods), its use may prove advantageous if periods of low signal-to-noise ratio are experienced.

It may prove to be more feasible to modify only the LM and S-IVB Synchronizers because of the following circumstances:

1. Since the additional circuitry is only employed during low transition densities (a non-existent case for the CSM) a modified S-IVB Synchronizer can be used as a back-up for LM or CSM; the S-IVB having the lowest priority.

^{*32} ones or 32 zeros

- 2. During low transition densities, D.C. restoration should be removed. It can be switched out of the Dynatronics equipment but not the Electro Mechanical Research equipment.
- 3. From Reference 2, which indicates the distribution of the two types of equipment in the MSFN, it is seen that enough Dynatronics equipment is available to implement two at each station. (One for LM and one for S-IVE). It is not known whether the redistribution of this equipment is practical.

V. Advantages and Disadvantages

The only readily apparent disadvantage (or problem area) is that associated with signal injection at the differentiating network before the 25.6 KHz VCO loop. It is one of keeping the injected signal from interfering with the data entering the decision circuitry. However, since the level will be constant at this point (except for noise) during periods of no transitions it may be isolated by a simple diode or transistor circuit and simply chopped at the normal data rate by the injected signal or the circuit could actually be broken at the time the coherent synchronization equipment is called into operation.

Some readily apparent advantages of the system modifications are:

- 1. The normal data stream through the decision circuitry is uninterrupted.
- 2. The additional equipment is only used when the bit density falls to a predetermined level. Thus, the system operates as it does presently until the LM special case arises.
- 3. LM, CSM, and S-IVB decommutating units can be implemented in the same manner making them interchangeable for backup purposes. Modified units accepting CSM and S-IVB data will not use the additional circuitry in data detection unless it is desirable for CSM realtime telemetry.
- 4. The additional equipment consists of, basically, "off-the-shelf" items--primarily counters.
- 5. The systems following the bit synchronizer need no modifications since they need not know the difference between a coherent and non-coherent synchronization of the timing reference.

VI. Consideration of Existing Equipment Modifications

Figure 5 shows the front panel of a typical bit synchronizer. Notice that the PCM output jack provides access for point C shown previously on Figures 2 and 3. Access for VCO signal injection will probably involve splitting the present PCM input jack. The only remaining access point required by the additional equipment is the 2.048 MHz VCO output in the telemetry subcarrier demodulator equipment.

VII. MSFN Tape Recording of Data

Having the VCO in synchronism at all times suggests that its output could be used to instill timing information on the PCM-C data be one tape recording. Furthermore, if this information were provided by making the data split-phase, the bit synchronizer could be simply switched to this condition (Figure 5) before playback. Figure 6 suggests such a method. From Reference 3, it is deduced that when two channels are available, both points B and C are monitored otherwise just point B. Thus, to implement in accordance with Figure 6, for all times, the channel normally recording B should be switched to record C. Note that having timing information available on the recorded data (only the PCM-C data is recorded presently) should prove useful for not only the above-mentioned equipment but also any other data processing equipment which might be used.

2034-WJB-dly

Attachments References Figures 1-6 W. J. Henden

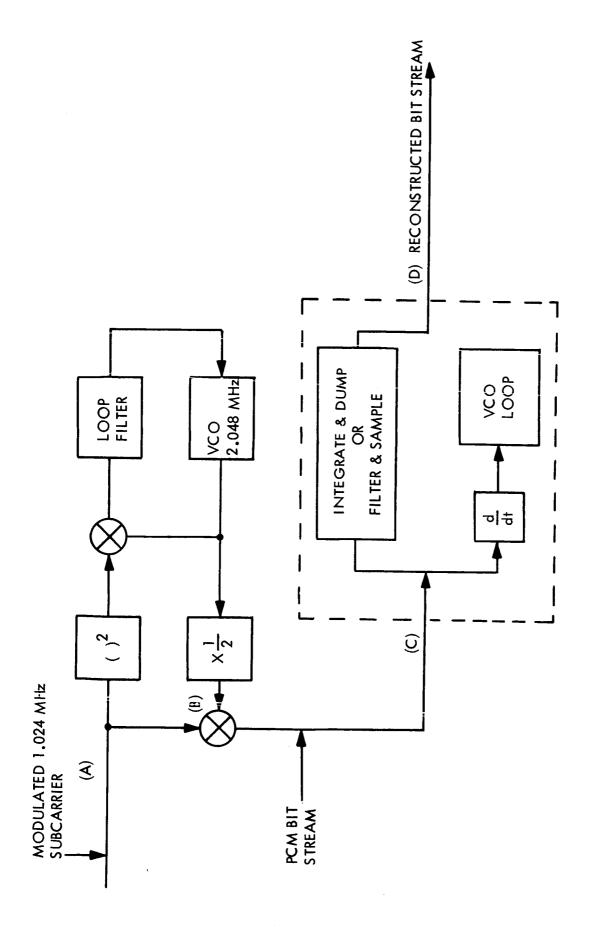


Figure 1. LM PCM-C data detection in the MSFN.

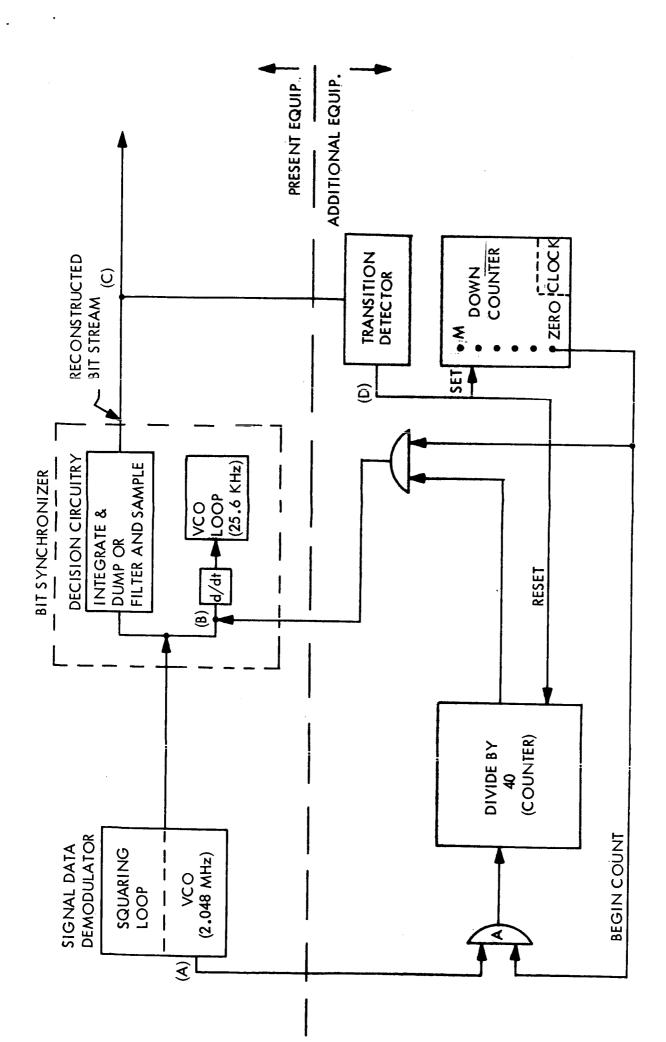


Figure 2. Possible method for maintaining Bit Sync during low transition densities (noncoherent clock)

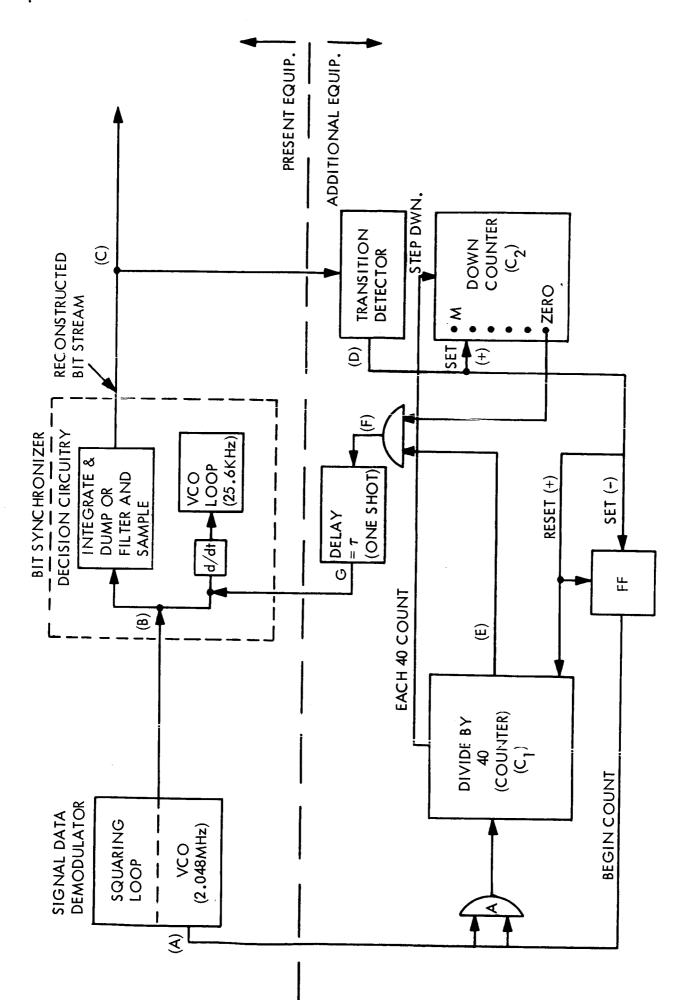


Figure 3. Possible method for maintaining Bit Sync during low transition densities (coherent clock)

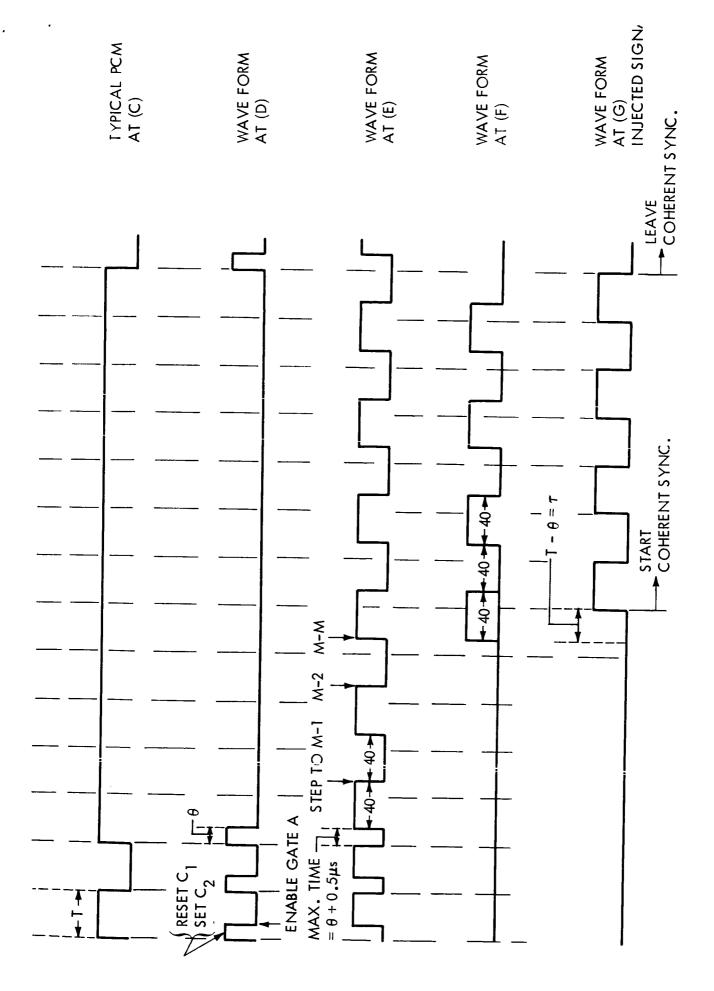


Figure 3A. Rough timing diagram for Figure 3.

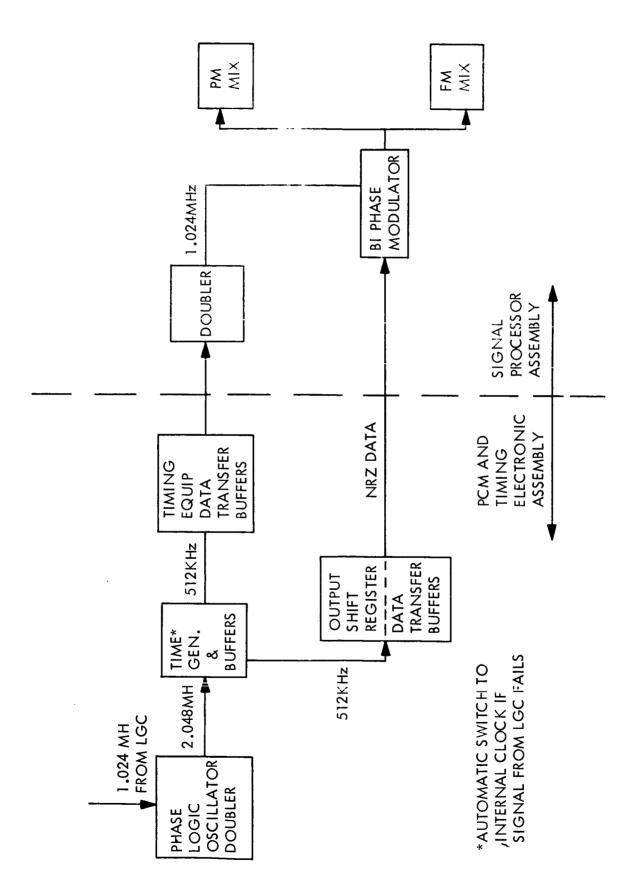


Figure 4. Diagram showing NRZ data being coherently related to the 1.024MHz subcarrier.

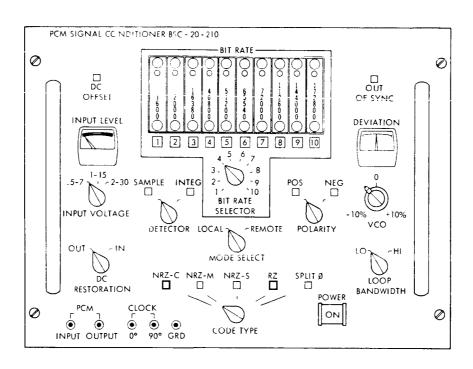


Figure 5 — Narrow band bit synchronizer

(FROM REFERENCE 1)

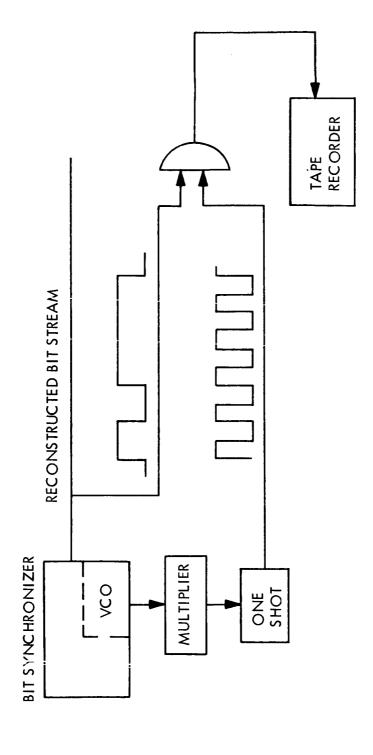


Figure 6. Possible implementation of timing on recorded data.

BELLCOMM, INC.

REFERENCES

- 1. Proceeding of the Apollo Unified S-Band Technical Conference, July, 1965 G. Hondros "Signal Data Demodulators," pp. 83-90 and W. A. Dentel "Apollo Network PCM Decomcutation Systems," pp. 165-178.
- 2. I and C Parel PCM Telemetry Group Report, Apollo PCM Link Compatibility, February 10, 1966, p. 14.
- 3. AS-204 Mission Supplements to Network Operations Directive for NASA Manned Space Flight Operations, November 1, 1966 Change 1, January 11, 1967, pp. 57-6 through 57-8.

BELLCOMM, INC.

Possible MSFN Solution to From: W. C. Benden Subject:

Loss of Bit Synchronization in LM PCM Telemetry

Case 320

Distribution List

NASA Headquarters

Messrs. J. K. Holcomb/MAO

T. A. Keegan/MA-2

J. T. McClanahan/MOR

L. M. Robinson/TS

J. D. Stevenson/MO

MSC

Messrs. R. H. Dietz/EE13

C. F. Herman/EB3

H. C. Kyle/EB

R. W. Morehead/EB2

L. Packham/EE

H. R. Rosenberg/EB2

P. Vavra/EB

GSFC

Messrs. D. A. Dalton/812

W. A. Dentel/812

Bellcomm

Messrs. A. P. Boysen, Jr.

R. K. Chen

D. R. Hagner

J. J. Hibbert

W. C. Hittinger

B. T. Howard

J. E. Johnson

E. J. Klein

H. Kraus

J. P. Maloy

J. Z. Menard

I. D. Nehama

B. F. O'Brien

T. L. Powers

J. T. Raleigh

MSFC

Messrs. T. A. Barr/R-ASTR-IR

J. T. Powell/R-ASTR-I

I. I. Rosenblum

I. M. Ross

J. A. Saxton

K. Schmid

N. W. Schroeder

L. Schuchman

R. L. Selden

B. P. Tunstall

R. L. Wagner

A. G. Weygand

W. D. Wynn

Department 1023

Central Files

Library